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RTL8125 Series

INTEGRATED 10/100/1000M/2.5G ETHERNET CONTROLLER FOR PCI EXPRESS APPLICATIONS

LAYOUT GUIDE

(CONFIDENTIAL: Development Partners Only)

Realtek CONFIDENTIAL for SYBA Tech Limited

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2018/03/30	First release.

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1. Introduction

The Realtek RTL8125 series of 10/100/1000M/2.5G Ethernet controller combine a multi-speed IEEE 802.3 compliant Media Access Controller (MAC) with a multi-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, the RTL8125 offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection and Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The RTL8125 supports the PCI Express 2.1 bus interface for host communications with power management, and complies with the IEEE 802.3u specification for 10/100Mbps Ethernet, the IEEE 802.3ab specification for 1000Mbps Ethernet, and the IEEE 802.3bz specification for 2.5Gbps Ethernet. It supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space. The RTL8125 features embedded One-Time-Programmable (OTP) memory.

Advanced Configuration Power management Interface (ACPI)—power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is supported to achieve the most efficient power management possible. PCI MSI (Message Signaled Interrupt) and MSI-X are also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet and Microsoft Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e., main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8125. To further reduce power consumption, the RTL8125 also supports PCIe L1 substate L1.1 and L1.2.

The RTL8125 supports 'RealWoW!' technology that enables remote wake-up of a sleeping PC through the Internet. This feature allows PCs to reduce power consumption by remaining in low power sleeping state until needed.

Note: The 'RealWoW!' service requires registration on first time use.

The RTL8125 is fully compliant with Microsoft NDIS5, NDIS6 (IPv4, IPv6, TCP, UDP) Checksum and Segmentation Task-offload (Large send and Giant send) features, and supports IEEE 802.1P Layer 2 priority encoding, IEEE 802.1Q Virtual bridged Local Area Network (VLAN) and IEEE 802.1ad Double VLAN.. The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

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The RTL8125 supports the ECMA (European Computer Manufacturers Association) proxy for sleeping hosts standard. The standard specifies maintenance of network connectivity and presence via proxies in order to extend the sleep duration of higher-powered hosts. It handles some network tasks on behalf of the host, allowing the host to remain in sleep mode for longer periods. Required and optional behavior of an operating proxy includes generating reply packets, ignoring packets, and waking the host.

The RTL8125 supports Receive Side Scaling (RSS) to hash incoming TCP connections and load-balance received data processing across multiple CPUs. RSS improves the number of transactions per second and number of connections per second, for increased network throughput.

The RTL8125 supports Virtual Machine Queue (VMQ) which is a hardware virtualization technology for the efficient transferring of network traffic to a virtualized host OS. The VMQ technology uses a hardware packet filter to deliver packets from an external virtual machine network directly to virtual machines; reducing the overhead of routing packets and copying from the management operating system to the virtual machine.

Note: The RTL8125 Virtual Machine Queue (VMQ) is only functional in computers running Windows Server 2008 R2 with the Hyper-V server role installed.

The RTL8125 supports IEEE 1588, IEEE 1588-2008, and IEEE 802.1AS, also known as Precision Time Protocol (PTP). IEEE 802.1AS is part of the Ethernet AVB (Audio Video Bridging) standard. PTP provides micro-second level accuracy time synchronization among multiple Ethernet devices. The RTL8125 implements hardware support for these standards. The RTL8125 supports IEEE 802.1Qav, also part of the Ethernet AVB standard. IEEE 802.1Qav is a forwarding and queuing mechanism enhancement. It provides guarantees for time-sensitive (i.e., bounded latency and delivery variation), loss-sensitive real-time audio video (AV) data traffic transmissions.

The RTL8125 supports IEEE 802.3az-2010, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az-2010 operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power.

The device also features inter-connect PCI Express technology. PCI Express is a high-bandwidth, low-pin-count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

The RTL8125 is suitable for multiple market segments and emerging applications, such as desktop, mobile, workstation, server, communications platforms, and embedded applications.

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2. Design and Layout

System designers should follow basic rules in layout and placement, general termination, power supply filtering, plane partitioning, and EMI reduction in order to optimize designs that use the RTL8125. Following these rules will greatly contribute to a properly functioning hardware system.

This guide has the following goals:

(1) Create a low-noise, power-stable environment.

(2) Reduce the degree of EMI/EMC and their influence on the RTL8125.

(3) Simplify the task of routing signal traces.

2.1. General Guidelines

In order to achieve maximum performance using the RTL8125, good design practices are required throughout the process. The following are some recommendations for implementing a high-performance system.

- Provide a good power source to the RTL8125. The power noise under normal operation must comply with the criteria in section 3.2.4 Measurement Criteria, page 11
- Verify that critical components such as the clock source and transformer meet application requirements
- Use de-coupling capacitors to reduce noise on the power and ground planes
- Keep de-coupling capacitors close to the RTL8125 (within 200 mils)
- Provide termination on all high-speed switching signals
- Use a smaller package for the capacitor to reduce the package inductance
- Use of 2 layer PCB is NOT recommended
- Avoid routing any signal traces on the ground plane or power plane

Use the following signal integrity techniques to reduce crosstalk:

- Shorter parallel routes
- Thinner dielectrics
- Proper termination
- Provide a solid ground plane
- Use the 3-W rule for parallel trace routes
- Use wide ground plane spacing

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2.2. Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible, meaning width, length, and location
- Avoid vias and layer changes if possible
- Keep transmit and receive pairs away from each other. Run orthogonally, or separate via a ground plane if possible
- Ninety-degree trace angles should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts

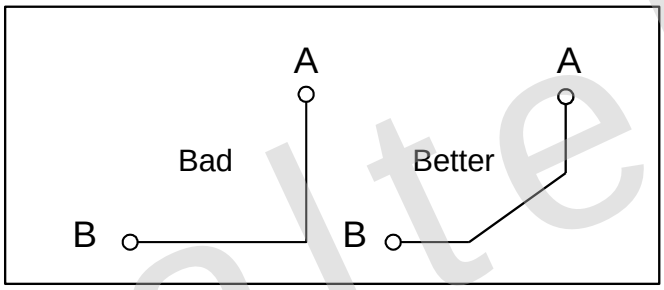

Figure 1. Signal Trace Angles

- Provide a solid ground plane reference as large and complete as possible and avoid discontinuities

2.3. Placing the RTL8125

- The RTL8125 should be placed as close as possible to the magnetics (less than 12cm).
- The resistor connected to the RSET pin should be placed close to the RSET pin (on the opposite side of the RSET pin is recommended, the distance should be less than 500 mils), and as far away as possible from signal traces and clock signals. The recommended minimum separation is 50 mils. The RSET resistor tolerance should < 1%. Ground shielding around the RSET resistor is needed.

2.4. Magnetics

- The magnetics should be placed as close to the RJ-45 connector as possible.
- The magnetics device, or devices with magnetic fields, should be separated and mounted at 90 degrees to each other
- There should be no power plane running under the RJ45/Magnetic/ICM.
- Center tap should be connected to 2.5V power rail directly to provide common mode for MDI signals.

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2.5. Crystal/Oscillator

- Following the 3W rule, the Crystal should be placed at least three times its own width from I/O ports, important or high frequency signal traces (Tx, Rx, and power), and magnetics, however, the clock trace lengths should be less than 2 inches long to reduce the current loop area
- Route crystal to the PHY directly. Traces should be kept as short and wide as possible with lengths less than 2 inches long. Avoid routing any high speed signal near the clock traces, any stub, or high speed signals near the clock signal traces
- The outer shield of the crystal requires good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, also need good grounding
- Place the oscillators toward the center of the PCB rather than near the edge. If the trace has to run along the edge of the board, make sure the trace to the board's edge distance is larger than the trace to a ground plane distance

2.6. Power Supply

- Power supply should be kept away from any MDI traces and RJ45/ICM to minimize any supply noise coupling. It is preferred that analog and digital supply planes do not cross one another.
- The gap between power planes on the same layer must be at least 15 mils. When power traces of different layers cross each other, the intersection should be 90 degrees.

2.7. Ferrite Beads and De-Coupling Capacitors

- Each PCB design has its unique noise coupling behavior. Ferrite beads could be used at the regulator output to suppress power noise. The voltage regulator output should be adjusted to guarantee the voltages measured at the power pins are sufficient, regardless of the voltage drop due to the ferrite beads
- Decoupling capacitors must be placed close to the power pins, such that the distance from the IC power pin to the capacitor is less than 200 mils

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3. Power Specification

3.1. Power Sequence

The power supply of the RTL8125 series should follow the power sequence specification below to ensure the internal circuits operate properly. If there is any action that involves consecutive ON/OFF toggling of the SWR source, the design must make sure the OFF state of both the SWR source and SWR output reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms. Note that the output DC level should fall within +/- 5% of the target voltage.

- Connect Pin 67 to the 0.9V power supply rail as an enable pin to ensure that the enable time of 0.9V would be well controlled by the RTL8125. The main objective is to ensure the 3.3V -> 2.5V -> 1.8V power sequence. Care must be taken that if different power modules are used for different power domains, the power rail output voltage sequence should be strictly maintained:

  3.3V power rail > 2.5V power rail > 1.8V power rail

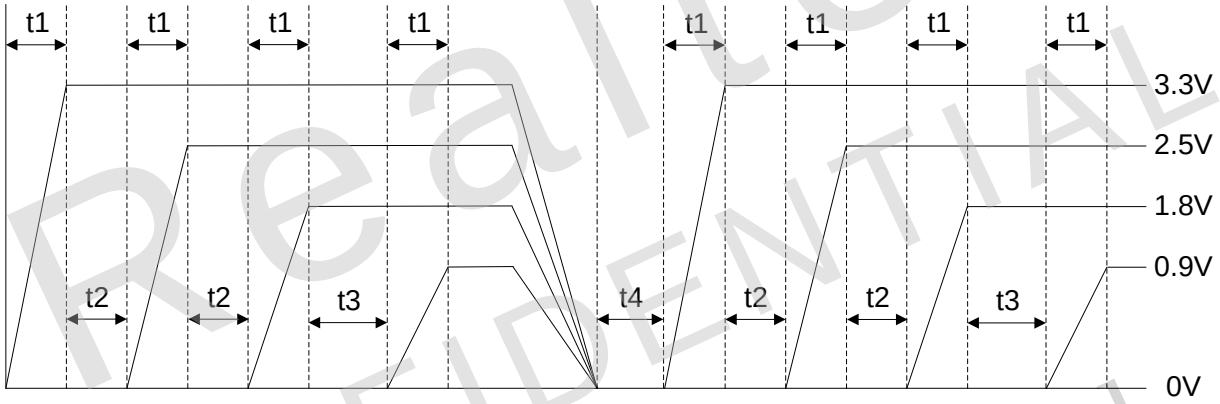

Figure 2. Power Sequence

Symbol	Description	Min	Typical	Max	Unit
t1	SWR Rise Time	0.5	1	10	ms
t2	SWR Enable Interval	-	-	-	ms
t3	1.8V to 0.9V Enable Interval*	-	-	-	ms
t4	On/Off Interval	50	-	-	ms

**. t3 should be well controlled by the RTL8125.*

Note that the output DC level tolerance is +/- 5% of the target voltage therefore the loosest counting of t1 would be the rising time required for power rail to output from 0V to 90% target voltage.

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0.5ms < Rise Time < 10ms and monotonic ramp

- No action to take.

0.1ms < Rise Time < 0.5 ms and monotonic ramp

- If the rise time is between 0.1ms~0.5ms and the power supply is in monotonic ramp, the customer MUST ensure that there is at least three times as much margin for inrush current to the RTL8125 so as to be safely under the system's power supply OCP threshold. For example: Assume customer supply power rise time of the RTL8125 is 0.374ms. The system power supply OCP is 9A. The inrush current of other devices is 5.64A. The inrush current to the RTL8125 must be less than 1.12A; otherwise an unanticipated system OCP may be triggered. It can be expressed in the following formula: Inrush current to the RTL8125 < (System power supply OCP - inrush current of other devices) / 3

Rise Time < 0.1 ms, or non-monotonic ramp

- Under this scenario, there is risk of an unanticipated ESD trigger event, which may cause permanent damage to the RTL8125. As well as an unanticipated ESD trigger event, the power supply source with rise time < 0.1ms or non-monotonic ramp may possibly cause permanent damage to the RTL8125. If there is any action that involves consecutive ON/OFF toggling of the power source, the design must make sure the OFF state of all power domain reach 0V, and the time period between the consecutive ON/OFF toggling action must be longer than 50ms.

3.2. Power Noise

In order to achieve maximum performance when using the RTL8125, a good power source should have power noise less than 30mV peak-to-peak for all power domains. If the power rail is supplied by SWR, then the SWR should operate in PWM (or CCM) mode to achieve this target. The details of power noise measurement including measurement points, measurement criteria, and setting of scope are illustrated in the following sections.

Note: The acceptable power noise peak to peak level given above is measured by specified instruments.

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3.2.1. Measurement Points

- 3.3V

  Measure each decoupling capacitor that is closest to each RTL8125 3.3V power pin. Include AVDD33, DVDD33 and potentially DVDD3318 (depends on POW_MODE1 configuration).

- 2.5V

  Measure each decoupling capacitor that is closest to each RTL8125 2.5V power pin. Include AVDD25 and DVDD25_UPS.

- 1.8V

  Measure each decoupling capacitor that is closest to each RTL8125 1.8V power pin. Include AVDD18, DVDD18, DVDD18_UPS and potentially DVDD3318 (depends on POW_MODE1 configuration).

- 0.9V

  Measure each decoupling capacitor that is closest to each RTL8125 0.9V power pin. Include AVDD09, DVDD09 and EVDD09.

To make power noise measure accurate, probe tip connections to decoupling capacitor should be short. We recommend probing the power noise directly on the PCB soldered pad, as shown in the following figures.

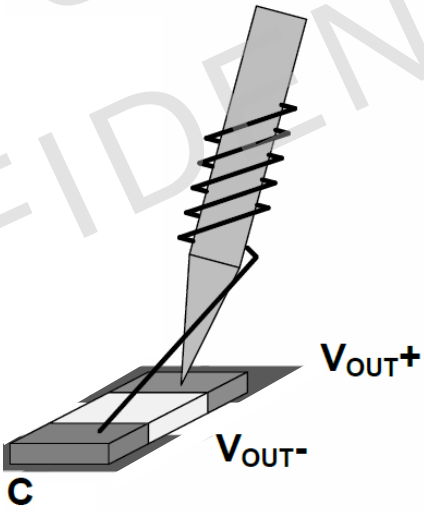

Figure 3. Power Noise Measure on Decoupling Capacitor (Using Coaxial Browser)

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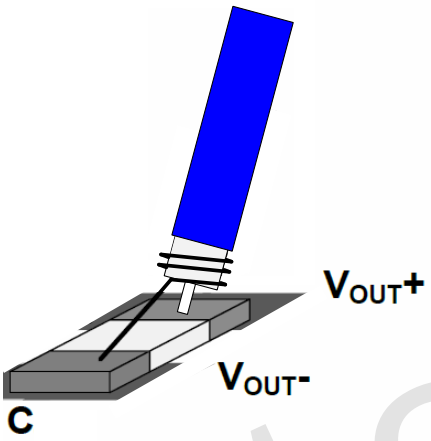

Figure 4. Power Noise Measure on Decoupling Capacitor (Using Pigtail Cable)

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3.2.2. Measurement Instrument

- Keysight N7020A power rail probe with 7023A (coaxial browser) or 7021A (pigtail cable)
- Keysight oscillator with bandwidth at lease 2GHz sampling rate and 2ms/ div time scale resolution ability

3.2.3. Measurement Setup

- Setup the scenarios:
  - Use the Keysight N7020A power rail probe together with an N7021A pigtail cable

    Solder the signal side of the pigtail cable to capacitor Vout+ side, and the ground side of the pigtail cable to capacitor Vout- side

    Connect the N7021A pigtail cable to the N7020A power rail probe, and then connect the N7020A to the Keysight scope (Probe calibration is needed before measuring)
  - Use the Keysight N7020A power rail probe together with an N7023A coaxial browser

    Connect the signal side of the coaxial browser to capacitor Vout+ side, and the ground side of the coaxial browser to capacitor Vout- side

    Connect the N7023A coaxial browser to the N7020A power rail probe, and then connect the N7020A to the Keysight scope (Probe calibration is needed before measuring)
- System Status
  - System Power: ON
  - Transmit/Receive Data at 2.5Gbps mode
- Acquisition Mode: Sample
- Vertical Scale/Resolution: 10mV/div
- Horizontal Scale
  - Time Scale/Resolution: 2ms/div
  - Sampling Rate: 2.5 GHz, 400ps/pt
  - Number of Acquisitions: 2000acqs at least
- Measurement Bandwidth: pigtail cable: 2GHz/ coaxial browser: 350MHz
- These settings are based on the following models of scope and probe
  - Keysight: DSOS404A, 4GHz
  - Keysight: N7020A Power Probe
- If a different model of scope or probe is used when doing the power noise measurement, ensure the scenario settings are as close as possible to those described above
- With the above scenarios and settings correctly done, the power noise measurement can be started

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3.2.4. Measurement Criteria

Power Noise Requirement under normal operation:

- Power Noise < 60mVpeak-to-peak when using coaxial cable (Figure 5)
- Power Noise < 30mVpeak-to-peak when using pigtail (Figure 6, page 12)

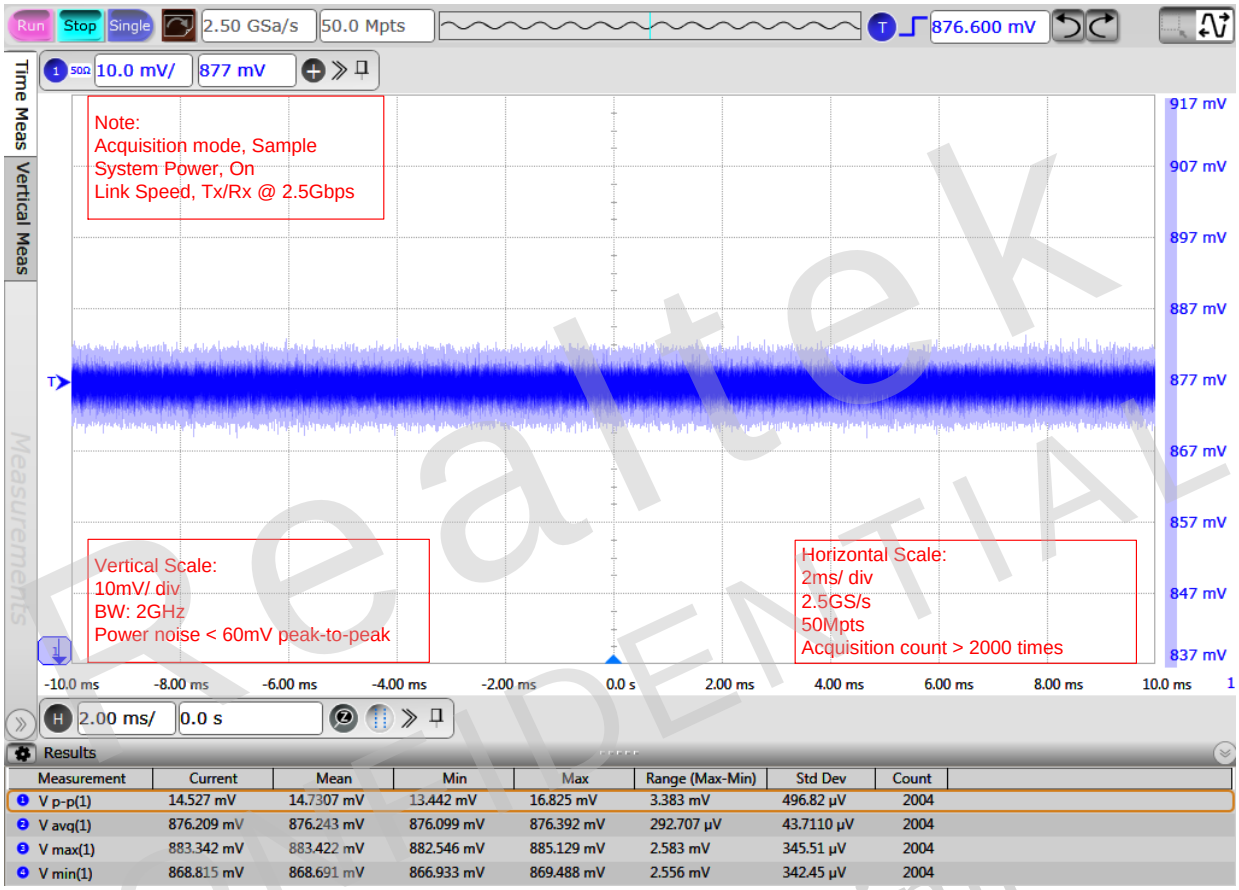

Figure 5. Power Noise Measure Result Using Coaxial Browser

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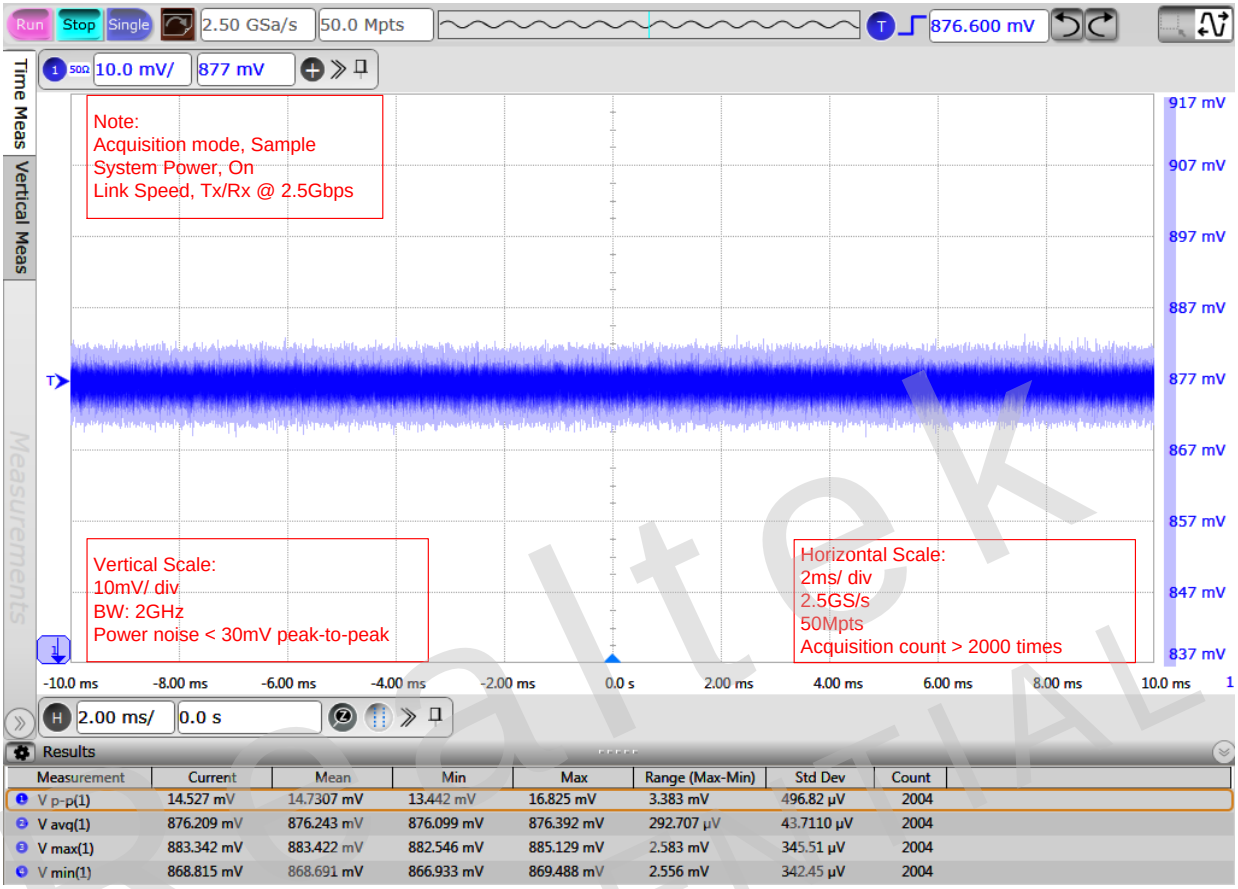

Figure 6. Power Noise Measure Result Using Pigtail

Note: The different peak-to-peak power noise criteria the between pigtail and coaxial browser is due to probe ability limitations. The pigtail measure should be closest to the true power noise seen by the RTL8125 thus we recommend this measure to determine the power noise. This does NOT imply the RTL8125 could withstand power noise over 30mV peak-to-peak during normal operation. If power noise is more than 30mV peak-to-peak measured by pigtail, the power noise level might lead the RTL8125 to malfunction.

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4. Signal and Trace Routing

Noise, ringing, and data lines should be controlled with proper termination. Power supply pins should be protected by proper filtering techniques. Good routing of traces can reduce propagation delay, crosstalk, and high frequency noise. It will also improve the signal quality to the receiver and reduce transmit signal losses.

- Ninety-degree trace corners should be avoided. We recommend that the traces turn at 45° angles as shown in Figure 1, page 4. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts
- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. It is better to have a power plane rather than power trace. If running power on the trace is unavoidable, the power supply breakout width should be wider than 15 mils, and properly filtered to minimize power noise effects. The clock and other high-speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a ground plane to surround them
- It is important to separate Digital Signals (e.g., EEPROM, SPI Flash) from Analog Signals (e.g., MDIP0/MDIN0, MDIP1/MDIN1, MDIP2/MDIN2, MDIP3/MDIN3, RSET) in order to avoid interference. If it is unavoidable to cross digital signals with analog power, do it at 90° angles
- RSET trace width is 6 mils (minimum) and is recommended to be isolated with a guard ground
- Differential pairs should have a continuous reference plane, and avoid vias. If vias are needed, MDI and PCIe signal vias should be of 10 mils width

  Avoid the following situations:

  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- Locate capacitors for coupled traces at the same location along the differential traces and near output pins of differential pairs)

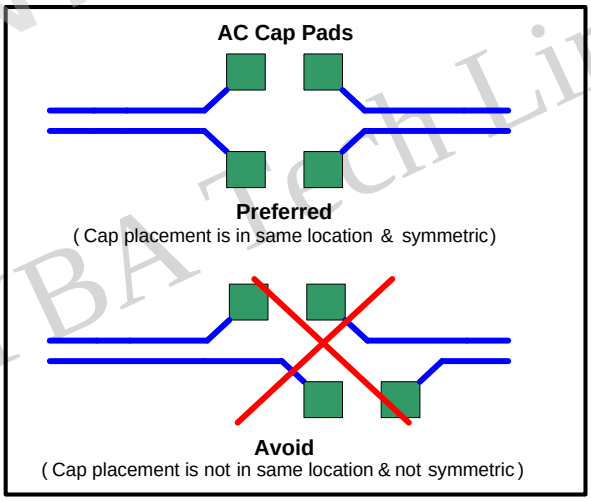
AC Cap Pads
Preferred
(Cap placement is in same location & symmetric)
Avoid
(Cap placement is not in same location & not symmetric)

Figure 7. Symmetrical Routing Into AC Capacitors

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4.1. MDI Signal Traces

- Traces routed from the RTL8125 to the 10/100/1000M/2.5G magnetics, and to the RJ-45 connector, should be as short as possible. The 12cm maximum length between the RTL8125 and magnetics is achievable only when there is no interference
- It is also very important to keep all four differential pair signal traces (MDIP0/MDIN0, MDIP1/MDIN1, MDIP2/MDIN2, MDIP3/MDIN3) at matching lengths (within 500mils). The positive and negative trace length difference must be less than 5 mils
- The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong canceling effect on noise. The width of D1 should be calculated to have 100Ω impedance (Figure 8). MDI impedance is 50ohm common mode; 100 ohm is differential mode

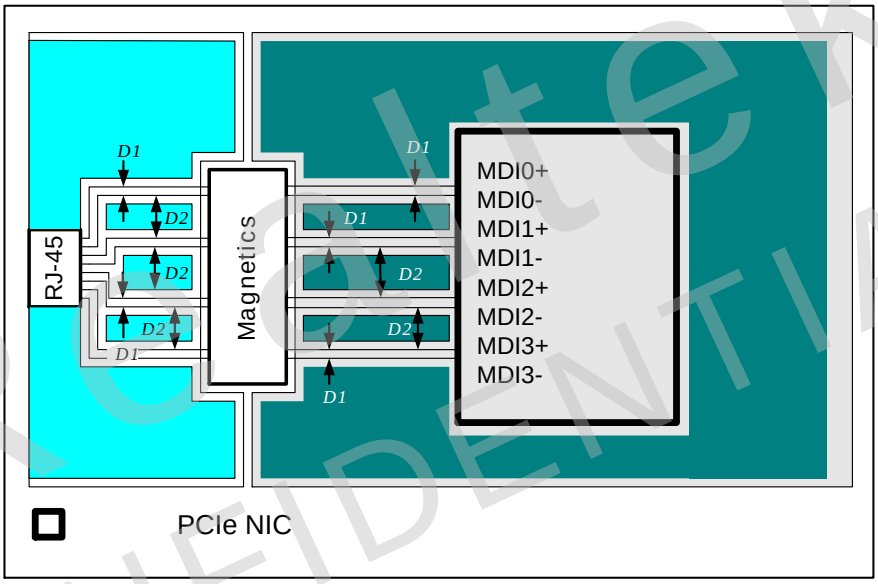

Figure 8. Signal & Trace Routing

- We suggest that there should be more than 30 mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2 in Figure 8). In addition, Ground Plane shielding can be used to separate all four signal pairs. However, a good layout should avoid the following situations:
  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, do not use vias on the four differential pairs (we recommend to place the four differential pairs on the same plane)

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- There should be a reference GND layer/plane (power plane should be avoided) under or above the MDI differential pairs signal layer. Signals crossing a plane split (see Figure 9) may cause unpredictable return path currents and would likely result in signal quality failure, as well as induce EMI problems

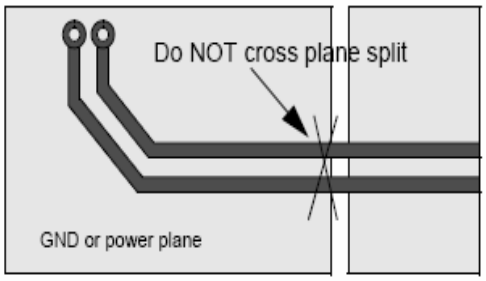

Figure 9. Signal Trace

4.1.1. MDI Swap

Some ICMs may have opposite A/B/C/D pin definition, which would increase the difficulty of MDI trace routing. As the result, RTL8125 support programmable ABCD to DCBA 4-pair reversal setting. The 4-pair reversal setting can help avoid the pair to pair signal traces crossing. Note that the pair reversal does NOT change the signal polarities

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4.2. Power Trace

- The power into the RTL8125 digital power pins can be improved with de-coupling capacitors. All analog power pins on the RTL8125 need to be de-coupled with a capacitor
- The vias of the de-coupling capacitor should be large enough in diameter. The de-coupling capacitors must be placed close to the RTL8125 (<200 mils), where power signal traces (de-coupling cap traces, power traces, grounding traces) should be as short and wide as possible
- It is better to have a power plane rather than power trace. If running power on the trace is unavoidable, the power supply breakout width should be wider than 15 mils, and properly filtered to minimize power noise effects

4.2.1. I/O Power Configuration

- The RTL8125 uses the POW_MODE1 pin to configure 3.3V or 1.8V as ISOLATEB, PERSTB, CLKREQB, LANWAKEB, GPI, and GPIO8 power. When POW_MODE1 pin is weakly pulled up to 3.3V, the operation voltage for ISOLATEB, PERSTB, CLKREQB, LANWAKEB, GPI, and GPIO8 is 1.8V. When POW_MODE1 pin is weakly pulled down to GND, the operation voltage is 3.3V
- Once I/O power voltage is configured via the POW_MODE1 pin, the corresponding voltage should be fed into DVDD3318 pins with a 0402 sized 0.1 µF capacitor placed near each DVDD3318 pin (<200 mils)

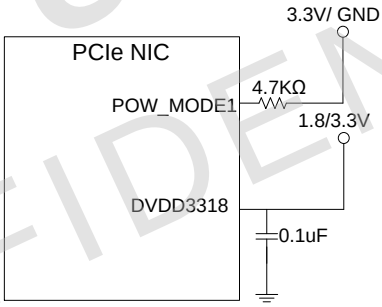

Figure 10. POW_MODE1_PIN Configuration (1.8V/3.3V)

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4.3. PCI Express Signal Trace

The PCI Express signal differential pairs should be 5 mils wide, with a spacing of 5 mils between them (REFCLK_P & REFCLK_N, HSOP & HSON, HSIP & HSIN). The length difference of the signals in a pair should not exceed 20 mils. For example, if HSON is 900 mils and HSOP is 850 mils, it may result in data transmit error.

PCI Express TX/RX differential pairs should comply with the following requirements:

- Differential Return Loss ≥ 10 dB (measured within a 50MHz~1.25GHz range)
- Differential Return Loss ≥ 8 dB (measured within a 1.25GHz~2.5GHz range)
- Common Mode Return Loss ≥ 6 dB (measured within a 50MHz~2.5GHz range)
- Differential Impedance should be maintained 85 ohm
- Only PCB traces are allowed for signal routing (do not use flat/shielded cable)
- There should be at least 50 mils spacing between different differential pairs, and they should be kept away from power or signal traces (at least 100 mils)
- All differential pair signals should maintain lateral routing symmetry between the two signals of a pair if possible. (see Figure 11 and Figure 12 below)

Figure 11. Symmetric Routing (Recommended)

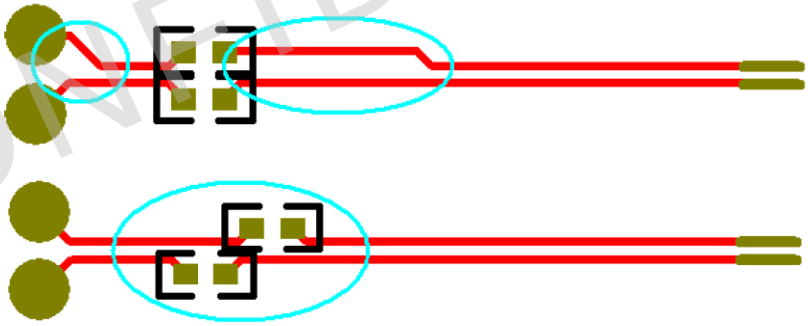

Figure 12. Asymmetric Routing (Avoid)

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5. Ground and Power Plane Layout

5.1. Ground Plane Layout

There is only one ground plane for analog power (AVDD33, AVDD25, AVDD18, AVDD09), digital power (DVDD33, DVDD25_UPS, DVDD18_UPS, DVDD09) and PCIE power (EVDD18, EVDD09). In the center of the IC, there is an Exposed Pad (EPAD) ground. The size of the center EPAD ground is 7.8mm x 7.5mm. The PCB layout requires at least 16 vias to connect the EPAD to the lower layer ground plane (see Figure 13).

Isolated separation between Analog and Digital Ground domains is not recommended since bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

Whether there is sufficient space on the PCB for an isolated separation layout must also be taken into consideration. The key point of such a layout is to keep the analog GND return path approximately equal to the common GND. If the system designer is not comfortable doing this, just place a single ground plane with no partition.

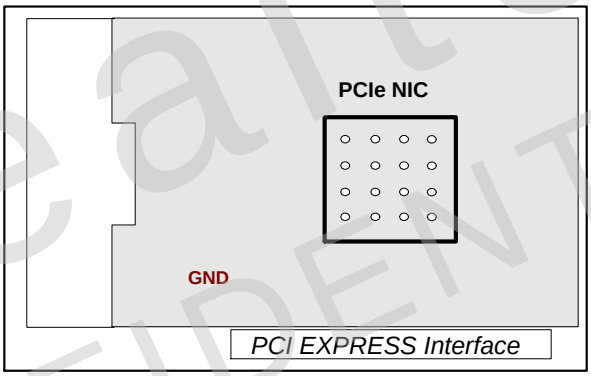

Figure 13. Ground Plane Layout-1

To achieve better ground plane performance, we recommend keeping the plane as large and uniform as possible. Figure 14 illustrates a not so good (left) and a good ground plane layout (right).

Figure 14. Ground Plane Layout-2

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The plane area beneath the magnetics should be left void. The void area is to keep transformer-induced noise away from the power and system ground planes (Figure 15).

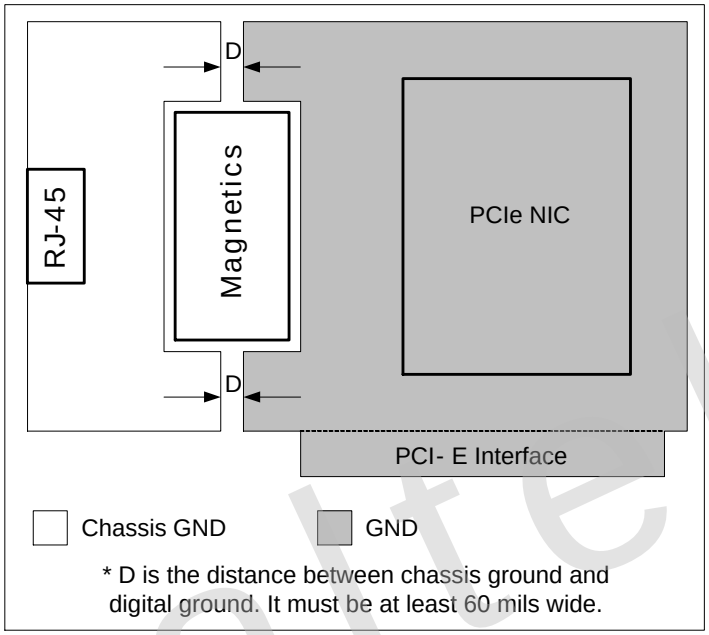

Figure 15. Ground Plane Separation

The Chassis Ground as shown in Figure 15 is known as an 'Isolated Ground'. It connects directly to the RJ-45 connector (fully shielded is recommended). In addition, 75ohm termination resistors and a 2kV (3kV recommended) high voltage capability capacitor between the magnetics RJ-45 jack side and the Chassis GND are needed for EMI and ESD protection.

It is also important to keep the gap (D in Figure 15) between Chassis GND and System GND wider than 60 mils for better isolation.

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5.2. Power Plane Layout

The digital power plane should be separated from analog areas, which are extremely sensitive to noise. We recommend using at least a 4-layer PCB.

Any analog circuitry on the same plane as the digital power will experience an energy fluctuation due to the fast switching time of digital components. A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. It is important to avoid using unnecessary power traces to the RTL8125, however, if it is unavoidable, try to keep these traces as short and wide as possible and make good use of vias.

(a) Decoupled Capacitor Example

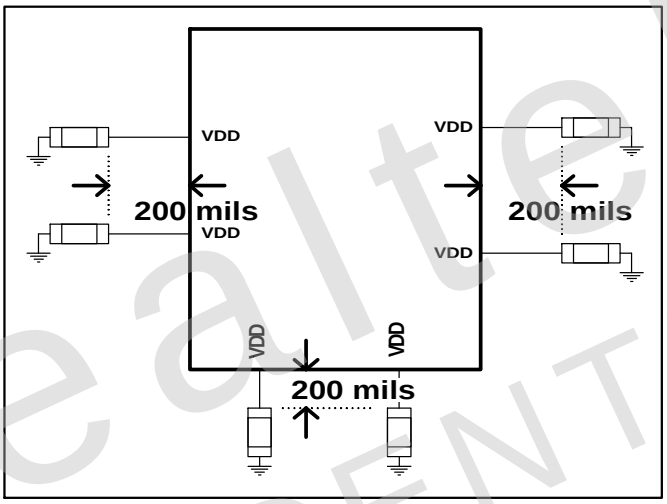

Figure 16. Decoupled Capacitor Example

(b) Use a Ferrite Bead or 0 ohm Resistor to Connect Digital and Analog Power

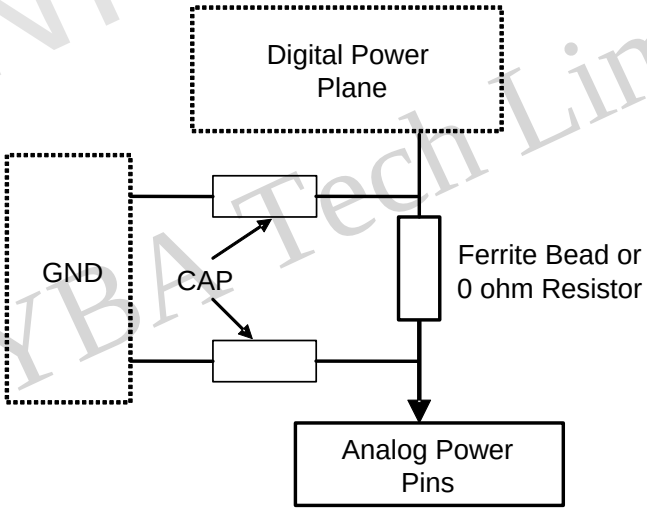

Figure 17. Power Plane

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To further improve the performance of the power plane, try to keep the contact area between the RTL8125 VDD pins and power plane as large as possible rather than using small narrow traces (Figure 18).

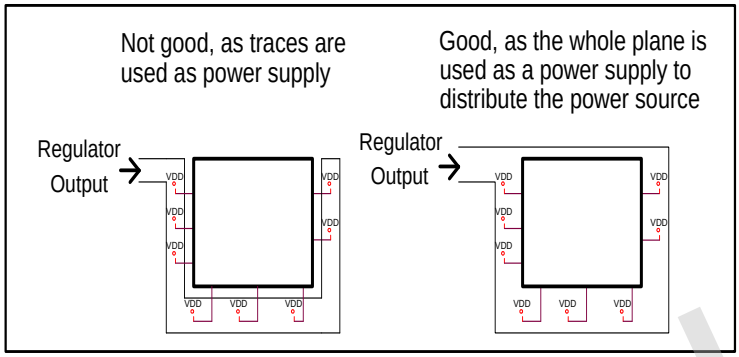
Not good, as traces are used as power supply
Good, as the whole plane is used as a power supply to distribute the power source
Regulator Output
Regulator Output
VDD

Figure 18. Power Source Distribution

- All 3.3V/2.5V/1.8V/0.9V decoupling capacitors shown in the reference schematic should be used in all designs
- Use 15 mils traces and 12 mils VIAs for the power supply breakouts
- The gap between power planes on the same layer must be at least 15 mils

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5.3. Four-Layer Board Plane Layout

1. Signal 1 (top layer)
2. GND
3. Power
4. Signal 2 (bottom)

5.3.1. Signal 1 Plane Layout (Top Layer)

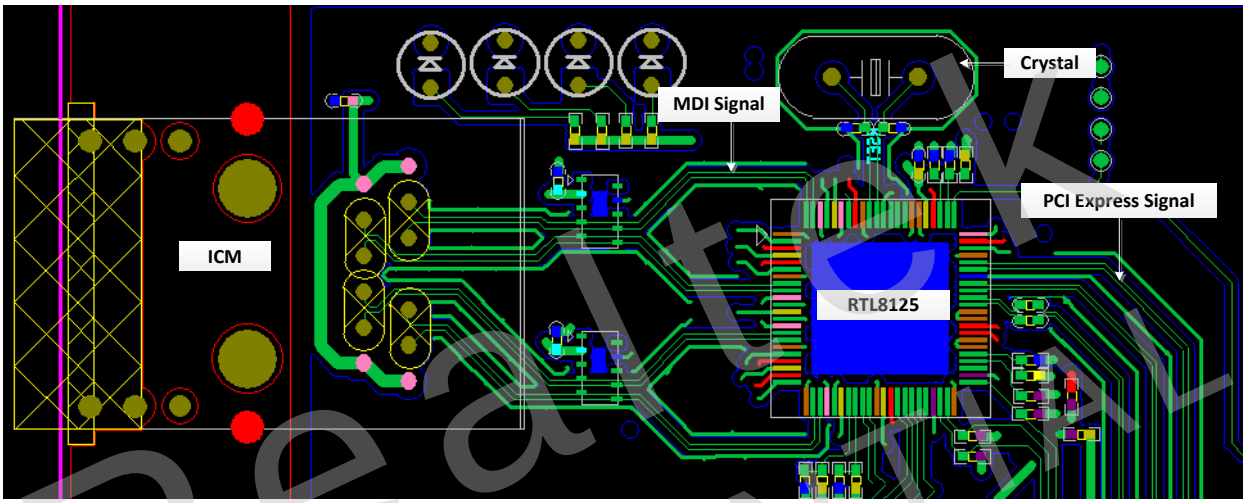

Figure 19. Signal 1 Plane Layout (Top Layer)

5.3.2. Ground Plane Layout (Layer 2)

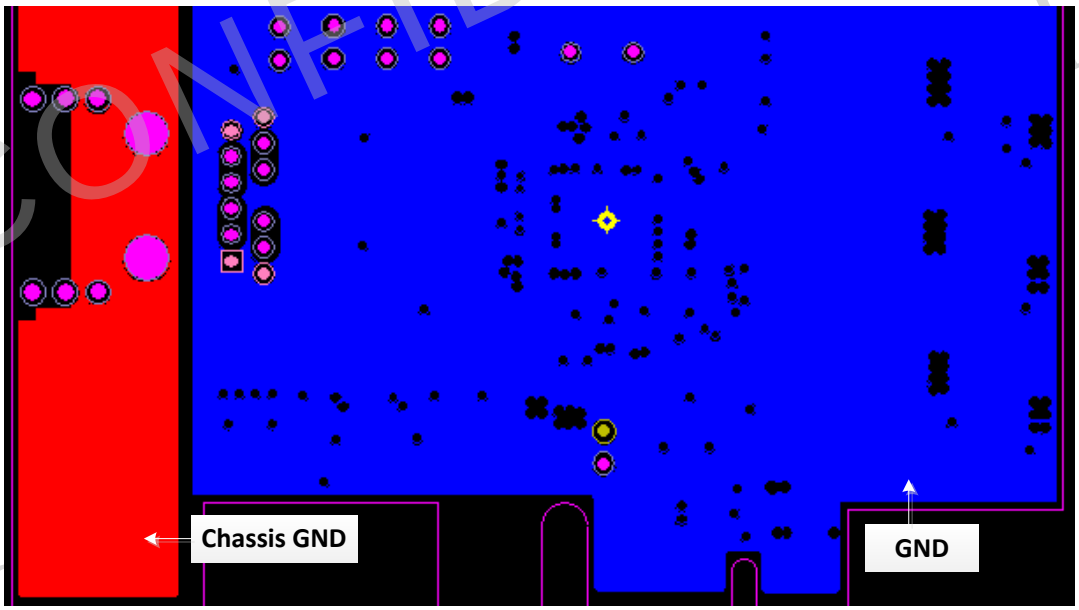

Figure 20. Ground Plane Layout (Layer 2)

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5.3.3. Power Plane Layout (Layer 3)

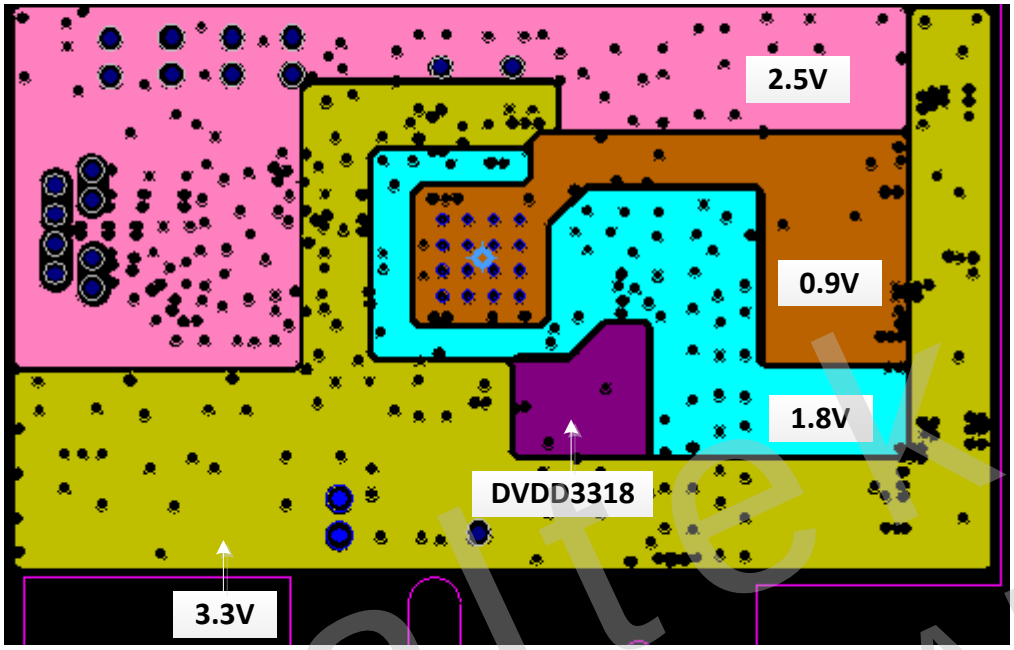

Figure 21. Power Plane Layout (Layer 3)

5.3.4. Signal 2 Plane Layout (Bottom Layer)

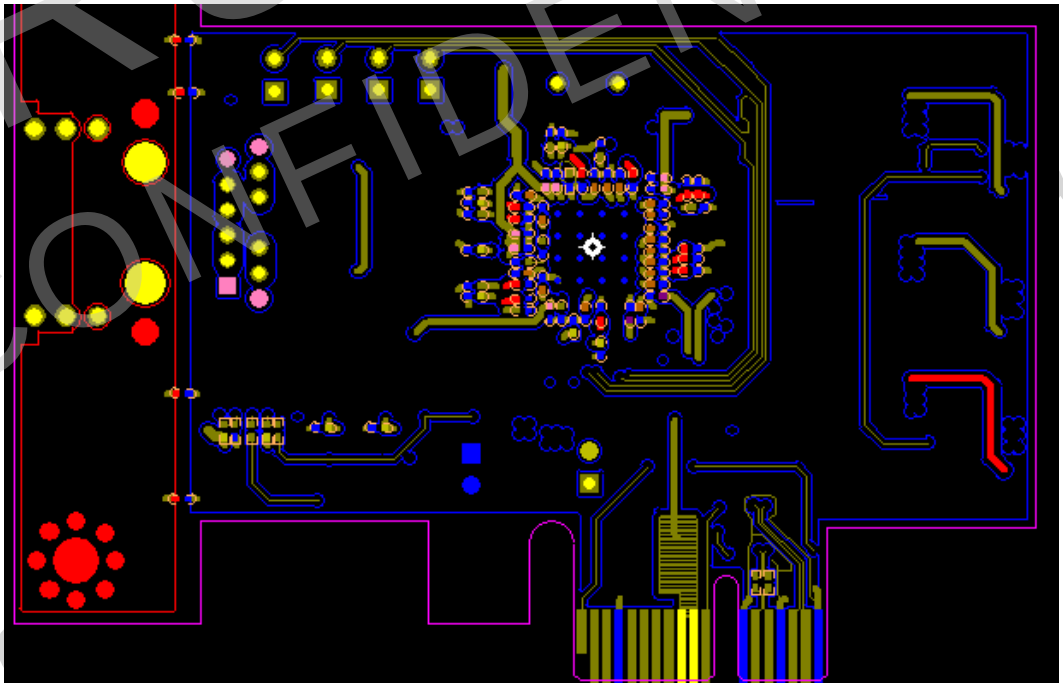

Figure 22. Signal 2 Plane Layout (Bottom Layer)

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6. Center-Tapping

- A center-tapped fine-tuned capacitor (C82 Value: 0.01µF~0.4µF) can improve EMI for single tone noise. The capacitor default is NC
- The Center tap should be connected to the 2.5V power rail directly to provide common mode for MDI signals.

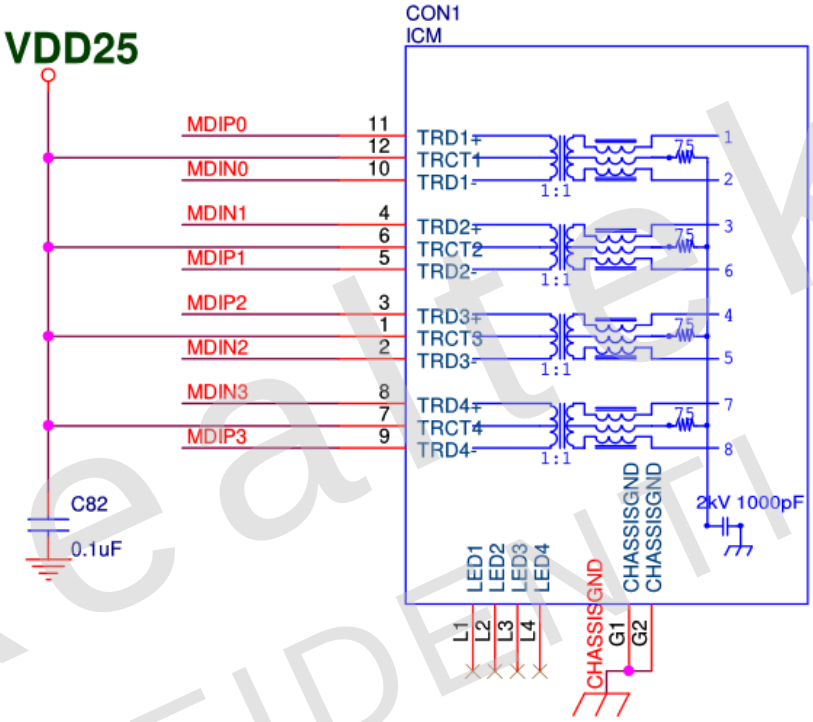

Figure 23. Center-Tapping

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- When using a separate transformer, the center-tap MUST be aggregated (pins 10, 7, 4, 1) (C84 Value: 0.01µF~0.4µF)

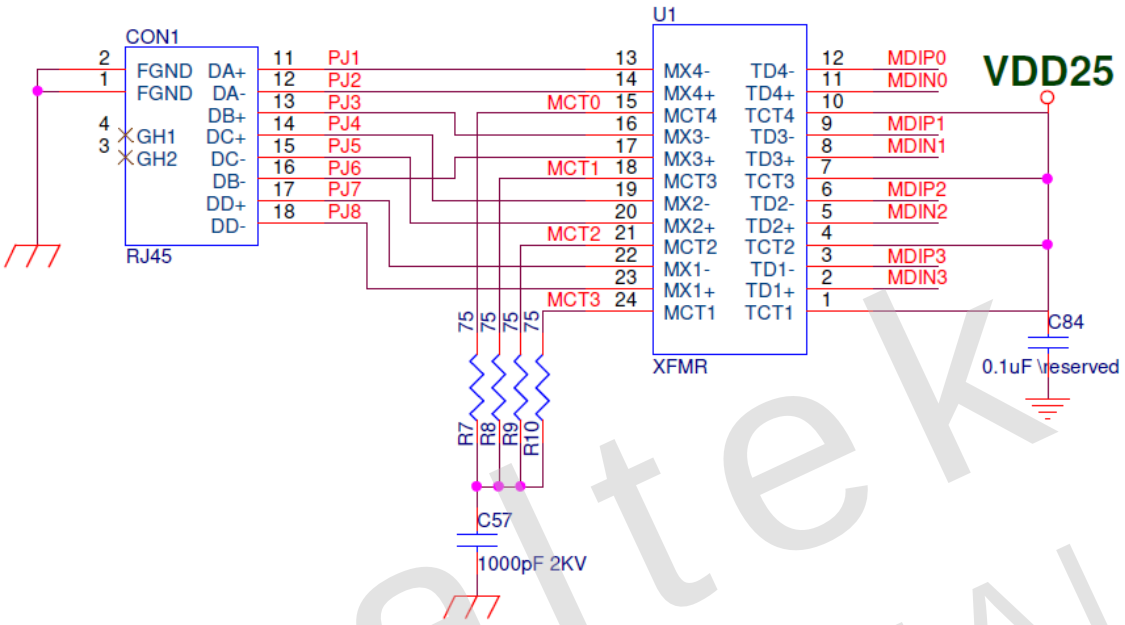

Figure 24. Separate Transformer

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7. Parts Recommendations

7.1. 10/100/1000M/2.5G Magnetics

Please contact Realtek FAE to get the ICM_XFMR_Available_Vendor_List for more information.

7.2. Reference Clock

A 25MHz parallel resonant crystal can be used as the reference clock source to replace the 25MHz Oscillator. The crystal must be connected to CKXTAL1 and CKXTAL2 pins. Shunt each crystal lead to ground with a 27pF capacitor.

Parameters	Range
Frequency	25MHz
Temperature Stability	±50ppm
Duty Cycle	50%±10%
Tolerance	±50ppm
ESR	Max 70Ω
Aging	5ppm/year, max.

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7.3. DC-DC Buck (Switching Regulator)

The power supplies have an important effect on the overall system performance, for power noise would propagate through power supply pins. We recommend the following criteria must be satisfied:

- Power noise should not exceed 30mv peak-to-peak.
- Switching frequency MUST be no less than 1MHz. Some SWR would enter PFM (or DCM) mode in light loading, which would lead to uncertain switching frequency. To prevent this uncertain noise couple into RTL8125 though power pins, SWR SHOULD operate in PWM (or CCM) mode.
- The power sequence described in the aforementioned section should be strictly followed. We recommend use SWR with EN pin and PG pin to implement the power sequence.
- Where ferrite beads are used between SWR and IC power pins, designers must ensure the voltage measured at the IC power pins are within the tolerance range in all application scenarios. That is, designers should take DCR of ferrite beads into consideration.
- Estimate the power dissipation for each power domain with 10% extra margin. For example, if a power domain consumes 1A in the worst case scenario, the SWR must be able to handle 1.1A loading. Please refer the power supply requirements listed below.

Power Domain	Supply Voltage Range	Worst Power Dissipation	Peak-to-Peak Power Noise	SWR Mode	SWR Switching Frequency
VDD33	3.3 +/- 5%	100mA	30mV peak-to-peak	PWM (or CCM)	No less than 1MHz in PWM mode
VDD25	2.5 +/- 5%	600mA			
VDD18	1.8 +/- 5%	600mA			
VDD09	0.9+/- 5%	1500mA			

NOTE: Power sequence should be 3.3V -> 2.5V -> 1.8V -> 0.9V

7.4. Resistors

Resistors that have tolerance requirements within 1% are recommended. Refer to the provided BOM for suggested schematics.

7.5. Ferrite Bead

The ferrite bead used should be of at least 100Ω@100MHz impedance with a rated current of 2A or higher.

7.6. RJ-45 Jack

A fully shielded RJ-45 connector should be used.

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8. Surge Protection

In order to provide adequate surge protection for the RTL8125, proper PCB design is required. The following are some recommendations for better surge protection of line-to-ground mode defined in the IEC-61000-4-5 specification.

8.1. General Guidelines

- There should be more than 30 mils spacing between different differential pairs of MDI signals. In addition, MDI signal trace routing between the magnetics and the RJ-45 connector should have clearance constraint from other traces with a minimum of 100 mils spacing
- Keep 75ohm termination resistors and high voltage capability capacitors away from other component pads (min 50 mils)
- For 75ohm termination resistors we recommend to use 0603 or larger resistors, with a maximum overload voltage specification of at least 100V
- Trace routing from the magnetics RJ-45 jack side through 75ohm termination resistors and a high voltage capability capacitor to the Chassis GND should be as wide as possible to make sure the whole discharge path is wide enough
    - The trace width should be more than 40 mils
    - Use at least 3 solder-filled blind vias (diameter ≥ 30 mils; drill size ≥ 20 mils) or a solder-filled through hole (diameter ≥ 60 mils; drill size ≥ 35 mils) if a layer change is needed

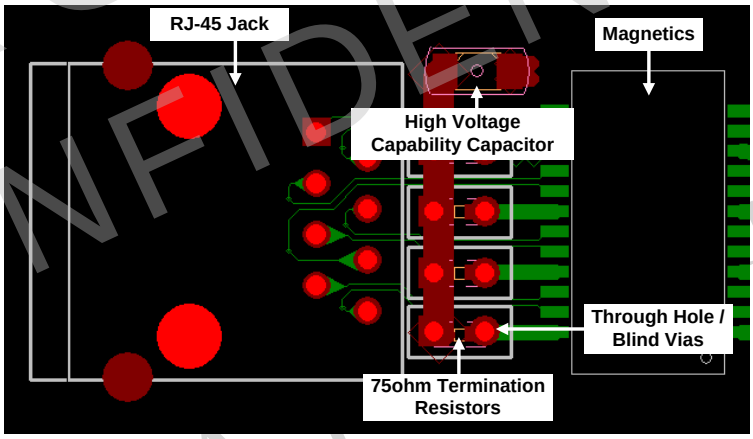

Figure 25. Trace Routing of the Magnetics RJ-45 Jack Side

- The power signal traces (power traces, ground traces) should be as short and wide as possible
- The plane area of the Chassis GND should be as large as possible. We recommend to have mounting screw holes on the board that connect the Chassis GND to the chassis

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8.2. Special Layout Technique

A low-cost PCB design technique for surge protection of line-to-ground mode developed by Realtek is the spark gap (Patent Pending), which can be implemented as a part of the component pattern of a PCB. The spark gap can produce spark discharge in a short gap and provide overvoltage protection from a surge event such as that produced by lightning transients.

- We suggest two spark gap pads that have half circles with a radius of 20 mils, and with a gap between each of 8 mils. The pads must not be covered with solder mask (copper exposure) and the gap area must be open to the air. The spark gap design is shown in Figure 26

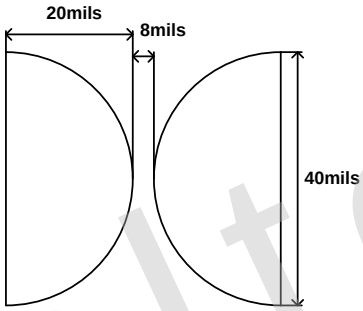

Figure 26. Spark Gap Design

- We recommend to place all spark gaps, 75ohm termination resistors, and a high voltage capability capacitor on the opposite side of the magnetics in the clear area, and keep these away from other component pads (minimum of 150 mils)
- The spark gap should be located between the source of the discharge path, e.g., the center tap of RJ-45 jack side of the magnetics, and the Chassis GND. The purpose is to generate a second discharge path and help to dissipate very high amplitude and fast rising surge voltage

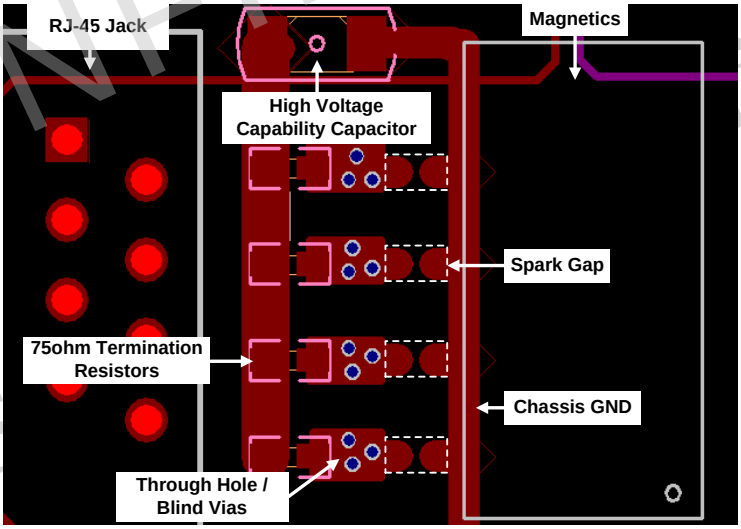

Figure 27. Spark Gap Layout

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9. Special Notes

The analog GND pins must maintain a good ground return path. To do this, avoid using single-ended grounds, enlarge the analog GND plane, and try to keep the analog circuit return back to the real GND (from PCI) as short as possible. This is particularly important for 10/100/1000M/2.5G Ethernet applications.

- If there is found to be a serious EMI issue, some de-coupling capacitors (0.01µF, 10µF) can be added between the system GND and power planes
- When using the oscillator as the clock source for 25MHz, avoid connecting any capacitors to the clock circuitry
- To achieve proper skew rate requirements, the digital bus traces for SPI flash and EEPROM should have lengths as equal as possible
- Keep a void area of at least 100 mils from the edge of each layer (e.g., power plane, GND plane, etc.) to the PCB edge in order to minimize fringe effect and lower EMI emissions

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